Announcements:

- HW3 solutions posted (discuss?)
- HW4: tonight (-ish)

Today:

- Profiling
- Program Representation

Timing Experiments: Pitfalls

What are potential issues in timing experiments? (What can you do about them?)

- Noise from users
- Timing noise
  - know clock sources
    - knowing your overheads
    - TSC
- Wait for the right things
- NUMA (pin mem & execution → core)
- Frequency scaling: RAPL → NUMA domain

Timing Experiments: Pitfalls (part 2)

What are potential issues in timing experiments? (What can you do about them?)

- uninitialized mem,

- alloc memory → calloc
- run a steam benchmark
- bandwidth > peak

Outline

Profiling: Basic Approaches

Measurement of "quantities" relating to performance

- Exact: Through binary instrumentation (valgrind/Intel Pin/...)
- Sampling: At *some* interval, examine the program state

We will focus on profiling by *sampling*.
Big questions:

- What to measure?
- At what intervals?

Defining Intervals: Performance Counters

A *performance counter* is a counter that increments every time a given event occurs.
What events?

- Demo: perf/Using Performance Counters
- see also Intel SDM, Volume 3

Interaction with performance counters:

- Read repeatedly from user code
- Interrupt program execution when a threshold is reached
- Limited resource!
  - Only a few available: 4-8 per core
  - Each can be configured to count one type of event
  - Idea: Alternate counter programming at some rate (requires steady-state execution!)

Profiling: What to Measure

- Raw counts are hard to interpret
- Often much more helpful to look at *ratios* of counts per core/subroutine/loop/...

What ratios should one look at?

Demo: perf/Using Performance Counters

Profiling: Useful Ratios

Basic examples:

- (Events in Routine 1)/(Events in Routine 2)
- (Events in Line 1)/(Events in Line 2)
- (Count of Event 1 in X)/(Count of Event 2 in X)

Architectural examples:

- IPC
- dTLB misses / (hits + misses)
- cache misses / instruction

/ clock

flops / ...

Issue with 'instructions' as a metric?

instructions ~ work?

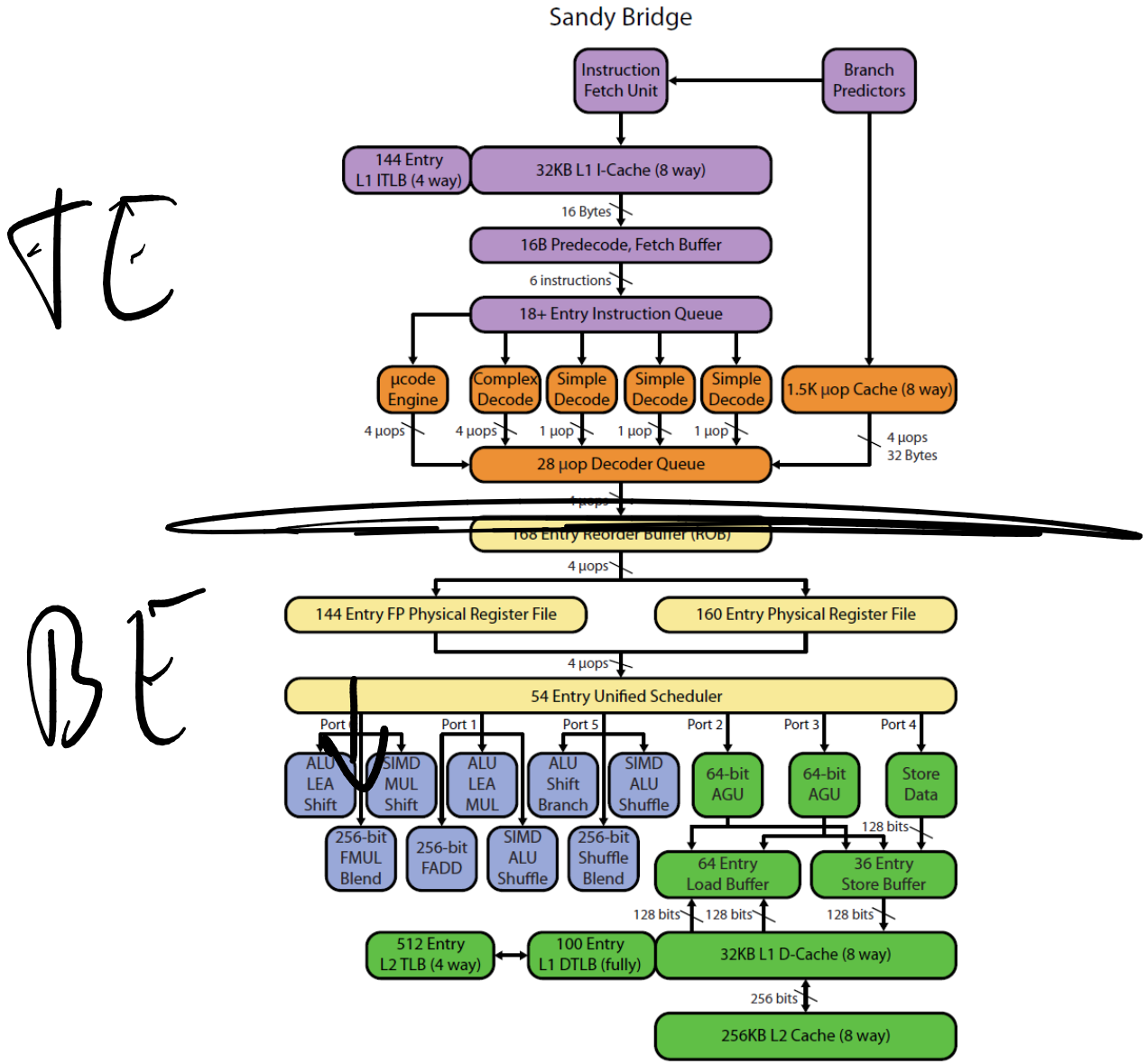
"Top-Down" Performance Analysis

Idea: Account for useful work per available issue slot

What is an issue slot?

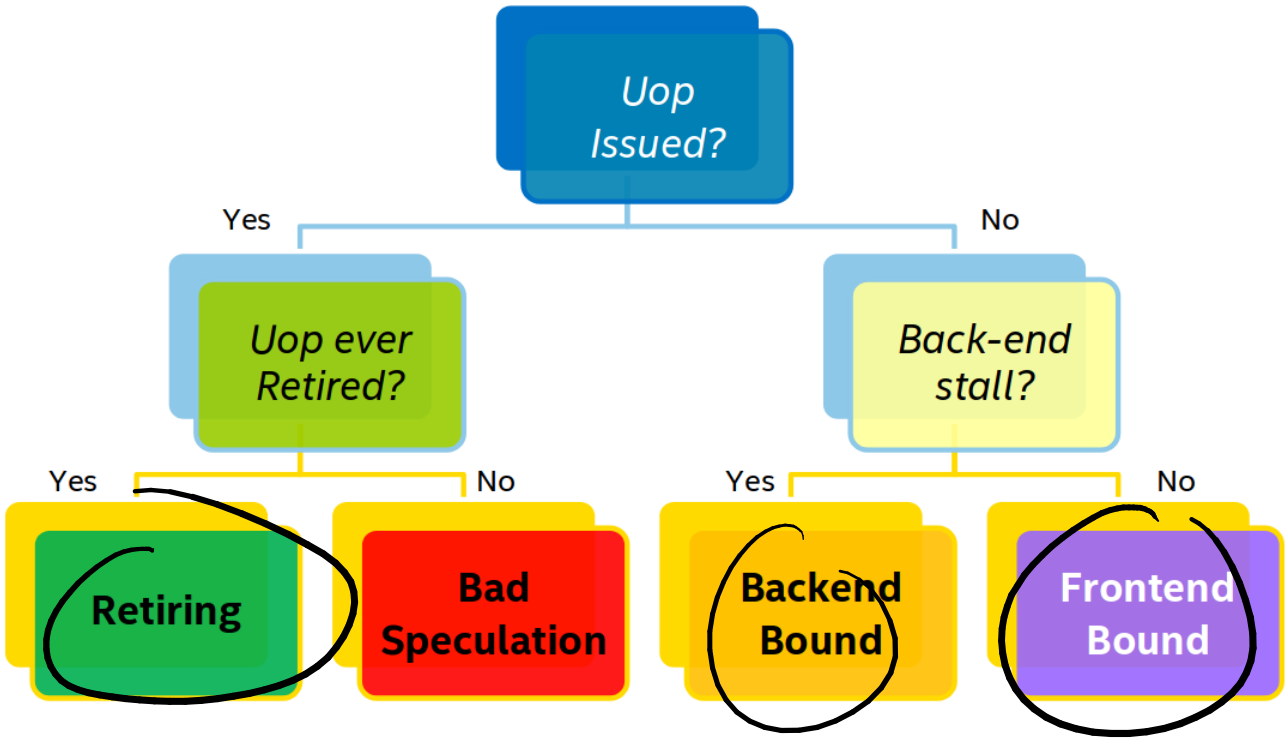
[Yasin '14]

Issue Slots: Recap



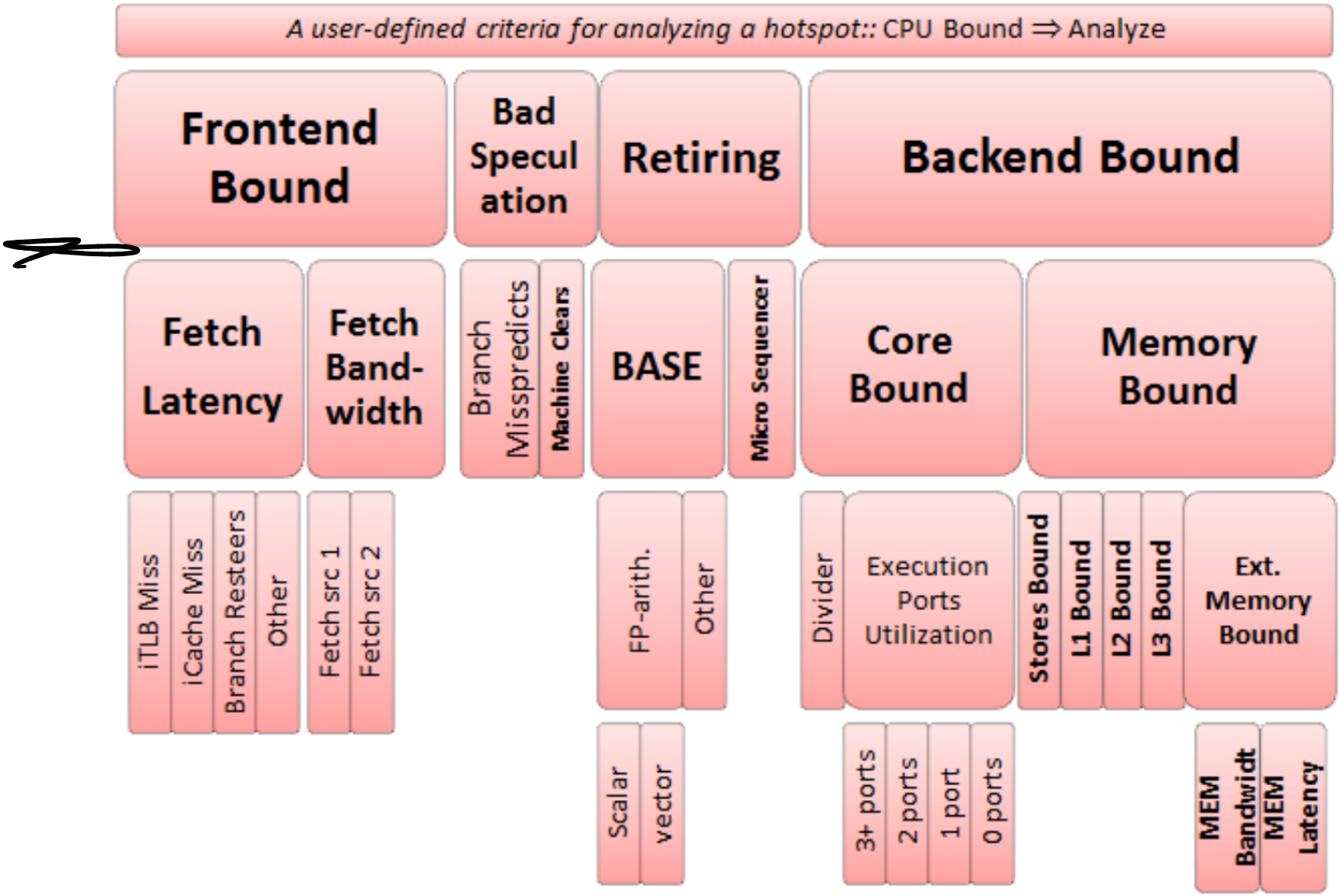
[David Kanter / Realworldtech.com]

What can happen to an issue slot: at a high level?



[Yasin '14]

What can happen to an issue slot: in detail?



[Yasin '14]

Outline

Demo: Performance Counters

Show the rest of:
Demo: perf/Using Performance Counters

Outline

Outline